74LVC377

Octal D-type flip-flop with data enable; positive-edge trigger

Rev. 05 — 21 February 2005 Product data sheet

1. General description

The 74LVC377 is a low-voltage, Si-gate CMOS device superior to most advanced CMOS compatible TTL families.

The 74LVC377 has eight edge-triggered D-type flip-flops with individual inputs (D) and outputs (Q). A common clock input (CP) loads all flip-flops simultaneously when data enable input ($\overline{E}$) is LOW. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Qn) of the flip-flop. Input $\overline{E}$ must be stable only one set-up time prior to the LOW-to-HIGH transition for predictable operation.

2. Features

- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- Direct interface with TTL levels
- Output drive capability 50 Ω transmission lines at 125 °C
- Complies with JEDEC standard:
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Quick reference data

Table 1: Quick reference data

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{PHL}, t_{PLH}	propagation delay CP to Qn	V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	-	4.6	-	ns
C_I	input capacitance		-	5.0	-	pF
f_{max}	maximum clock frequency	V_{CC} = 3.3 V	-	330	-	MHz

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Table 1: Quick reference data *…continued*

GND = 0 V; T_{amb} = 25 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{PD}	power dissipation capacitance per flip-flop		[1] [2]	-	22	-	pF

[1] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[2] The condition is V_I = GND to V_{CC}.

4. Ordering information

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC377D	–40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74LVC377DB	–40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74LVC377PW	–40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

5. Functional diagram

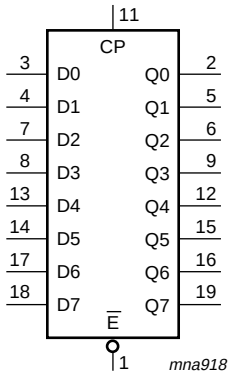


Fig 1. Logic symbol

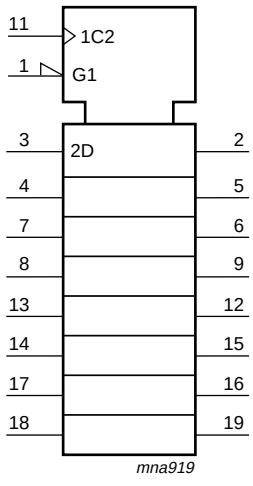


Fig 2. IEC logic symbol

6. Pinning information

6.1 Pinning

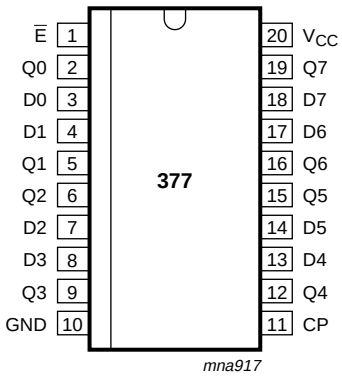


Fig 3. Pin configuration SO20 and (T)SSOP20

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
$\overline{E}$	1	data enable input (active LOW)
Q0	2	flip-flop output 0
D0	3	data input 0
D1	4	data input 1
Q1	5	flip-flop output 1
Q2	6	flip-flop output 2
D2	7	data input 2
D3	8	data input 3
Q3	9	flip-flop output 3
GND	10	ground (0 V)
CP	11	clock input (LOW-to-HIGH; edge-triggered)
Q4	12	flip-flop output 4
D4	13	data input 4
D5	14	data input 5
Q5	15	flip-flop output 5
Q6	16	flip-flop output 6
D6	17	data input 6
D7	18	data input 7
Q7	19	flip-flop output 7
V_{CC}	20	power supply

7. Functional description

7.1 Function table

Table 4: Function table [1]

Operating mode	Control		Input	Output
	CP	$\overline{E}$	Dn	Qn
Load 1	↑	l	h	H
Load 0	↑	l	l	L
Hold	↑	h	X	no change
Do nothing	X	H	X	no change

[1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition;
↑ = LOW-to-HIGH CP transition;
X = don t care.

8. Limiting values

Table 5: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+6.5	V
V_I	input voltage		[1]	–0.5	+5.5	V
V_O	output voltage		[1]	–0.5	V_{CC} + 0.5	V
I_{IK}	input diode current	V_I < 0 V		-	–50	mA
I_O	output source or sink current	V_O = 0 V to V_{CC}		-	±50	mA
I_{OK}	output diode current	V_O > V_{CC} or V_O < 0 V		-	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current			-	±100	mA
T_{stg}	storage temperature			–65	+150	°C
P_{tot}	total power dissipation	T_{amb} = –40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO20 packages: above 70 °C derate linearly with 8 mW/K.
For (T)SSOP20 packages: above 60 °C derate linearly with 5.5 mW/K.

9. Recommended operating conditions

Table 6: Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	maximum speed performance	2.7	-	3.6	V
		low-voltage applications	1.2	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	–40	-	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 1.2 V to 2.7 V	0	-	20	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

10. Static characteristics

Table 7: Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	GND	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = –100 µA; V_{CC} = 2.7 V to 3.6 V	V_{CC} – 0.2	V_{CC}	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	V_{CC} – 0.5	-	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	V_{CC} – 0.6	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	V_{CC} – 0.8	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.7 V to 3.6 V	-	-	0.2	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.4	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.55	V
I_{LI}	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	±0.1	±5	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; V_I = V_{CC} or GND; I_O = 0 A	-	0.1	10	µA
ΔI_{CC}	additional quiescent supply current	V_{CC} = 2.7 V to 3.6 V; V_I = V_{CC} – 0.6 V; I_O = 0 A	-	5	500	µA
C_I	input capacitance		-	5.0	-	pF
T_{amb} = –40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	GND	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	V

Table 7: Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = –100 µA; V_{CC} = 2.7 V to 3.6 V	V_{CC} – 0.3	V_{CC}	-	V
		I_O = –12 mA; V_{CC} = 2.7 V	V_{CC} – 0.65	-	-	V
		I_O = –18 mA; V_{CC} = 3.0 V	V_{CC} – 0.75	-	-	V
		I_O = –24 mA; V_{CC} = 3.0 V	V_{CC} – 1	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 100 µA; V_{CC} = 2.7 V to 3.6 V	-	-	0.3	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	-	0.6	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	-	0.8	V
I_{LI}	input leakage current	V_{CC} = 3.6 V; V_I = 5.5 V or GND	-	-	±20	µA
I_{CC}	quiescent supply current	V_{CC} = 3.6 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	-	40	µA
ΔI_{CC}	additional quiescent supply current	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC}$ – 0.6 V; I_O = 0 A	-	-	5	mA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8: Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 6.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{amb} = –40 °C to +85 °C [1]							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 4					
		V_{CC}= 1.2 V		-	15.0	-	ns
		V_{CC} = 2.7 V		1.5	4.9	7.9	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.5	4.6	7.6	ns
t_W	clock pulse width HIGH or LOW	see Figure 4					
		V_{CC}= 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		5.0	1.6	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	4	1.0	-	ns
t_{su}	set-up time						
	$\overline{E}$ to CP	see Figure 5					
		V_{CC} = 1.2 V		-		-	ns
		V_{CC} = 2.7 V		5.0	0.6	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	3	0.2	-	ns
	Dn to CP	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		3.0	1.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	2.0	0.7	-	ns

Table 8: Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 6.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_h	hold time $\overline{E}$ to CP						
	$\overline{E}$ to CP	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		0	–1.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	[2]	1.0	0	-	ns
	Dn to CP	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		0	–1.1	-	ns
		V_{CC} = 3.0 V to 3.6 V		0	–1.0	-	ns
f_{max}	maximum clock frequency	see Figure 4					
		V_{CC} = 1.2 V		-	-	-	MHz
		V_{CC} = 2.7 V		150	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[2]	150	330	-	MHz
$t_{sk(0)}$	skew	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.0	ns
C_{PD}	power dissipation capacitance per flip-flop		[4] [5]	-	22	-	pF
T_{amb} = –40 °C to +125 °C							
t_{PHL}, t_{PLH}	propagation delay CP to Qn	see Figure 4					
		V_{CC}= 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		1.5	-	10	ns
		V_{CC} = 3.0 V to 3.6 V		1.5	-	9.5	ns
t_W	clock pulse width HIGH or LOW	see Figure 4					
		V_{CC}= 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		5.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		4.0	-	-	ns
t_{su}	set-up time						
	$\overline{E}$ to CP	see Figure 5					
		V_{CC} = 1.2 V		-		-	ns
		V_{CC} = 2.7 V		5.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		3.0	-	-	ns
	Dn to CP	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		3.0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		2.0	-	-	ns

Table 8: Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 6.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_h	hold time $\overline{E}$ to CP						
	$\overline{E}$ to CP	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		1.0	-	-	ns
	Dn to CP	see Figure 5					
		V_{CC} = 1.2 V		-	-	-	ns
		V_{CC} = 2.7 V		0	-	-	ns
		V_{CC} = 3.0 V to 3.6 V		0	-	-	ns
f_{max}	maximum clock frequency	see Figure 4					
		V_{CC} = 1.2 V		-	-	-	MHz
		V_{CC} = 2.7 V		150	-	-	MHz
		V_{CC} = 3.0 V to 3.6 V		150	-	-	MHz
$t_{sk(0)}$	skew	V_{CC} = 3.0 V to 3.6 V	[3]	-	-	1.5	ns

[1] Typical values are measured at T_{amb} = 25 °C.

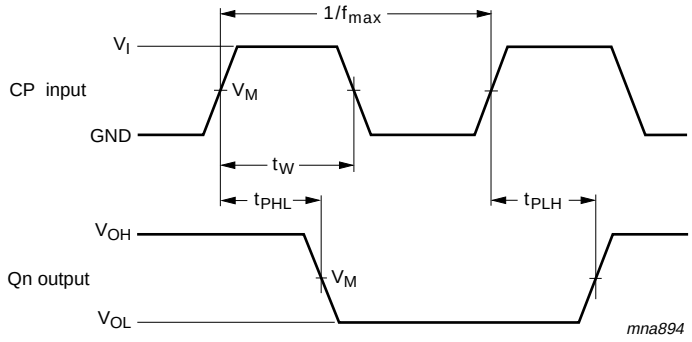
[2] Typical value is measured at V_{CC} = 3.3 V.

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

[5] The condition is V_I = GND to V_{CC}.

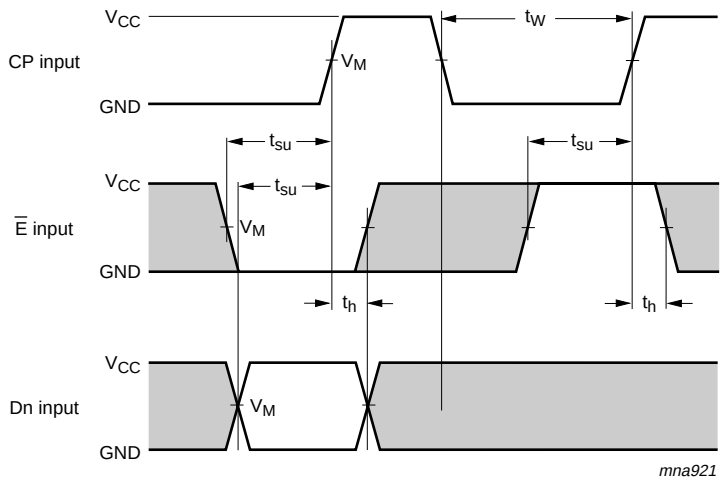
12. Waveforms



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig 4. Propagation delay clock (CP) to output (Qn), pulse width clock (CP) and maximum clock pulse frequency



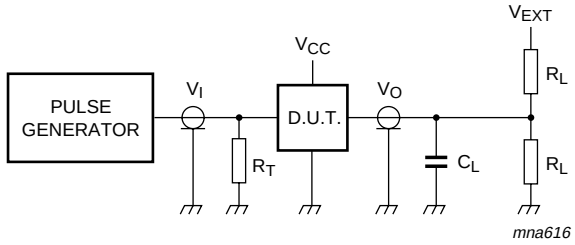
Measurement points are given in Table 9.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 5. Data set-up and hold times of data input (Dn) and enable input ($\overline{E}$) and pulse width of enable input ($\overline{E}$)

Table 9: Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.2 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistor.

V_{EXT} = Test voltage for switching times.

Fig 6. Load circuitry for switching times

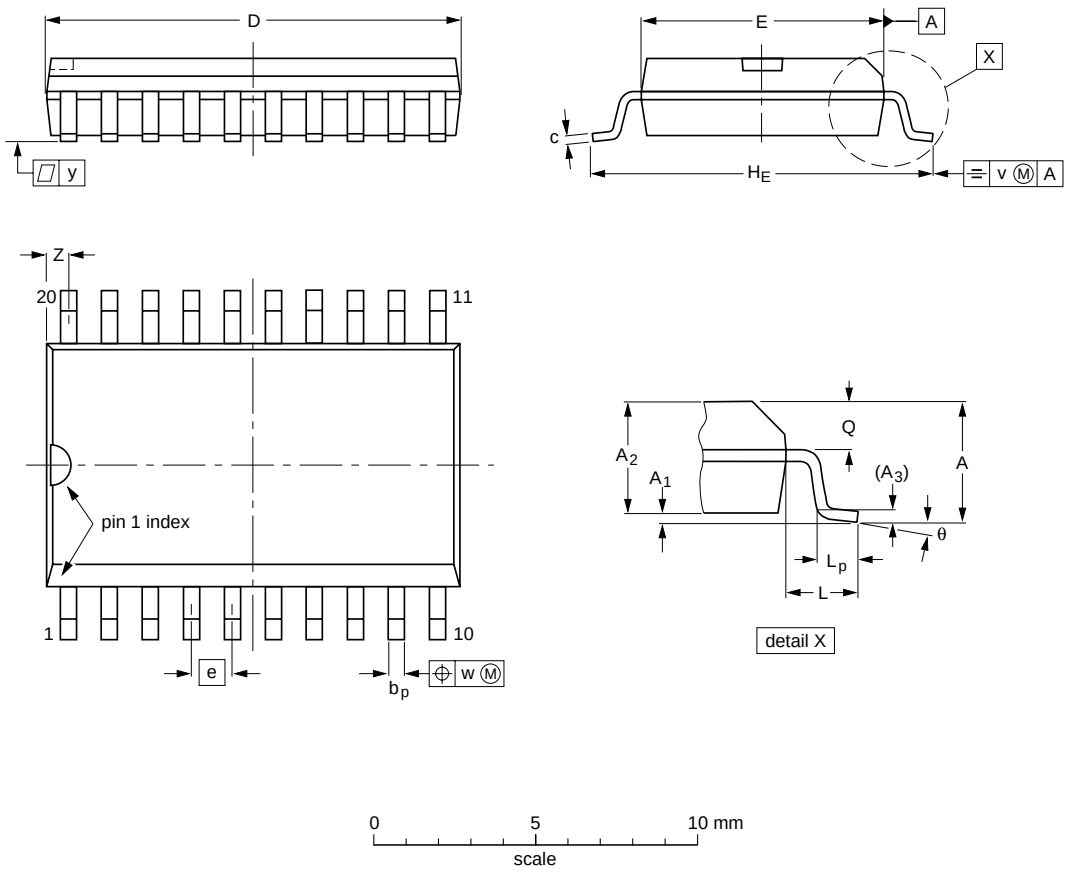
Table 10: Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}
1.2 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω [1]	open
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open

[1] The circuit performs better when R_L = 1000 Ω.

13. Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

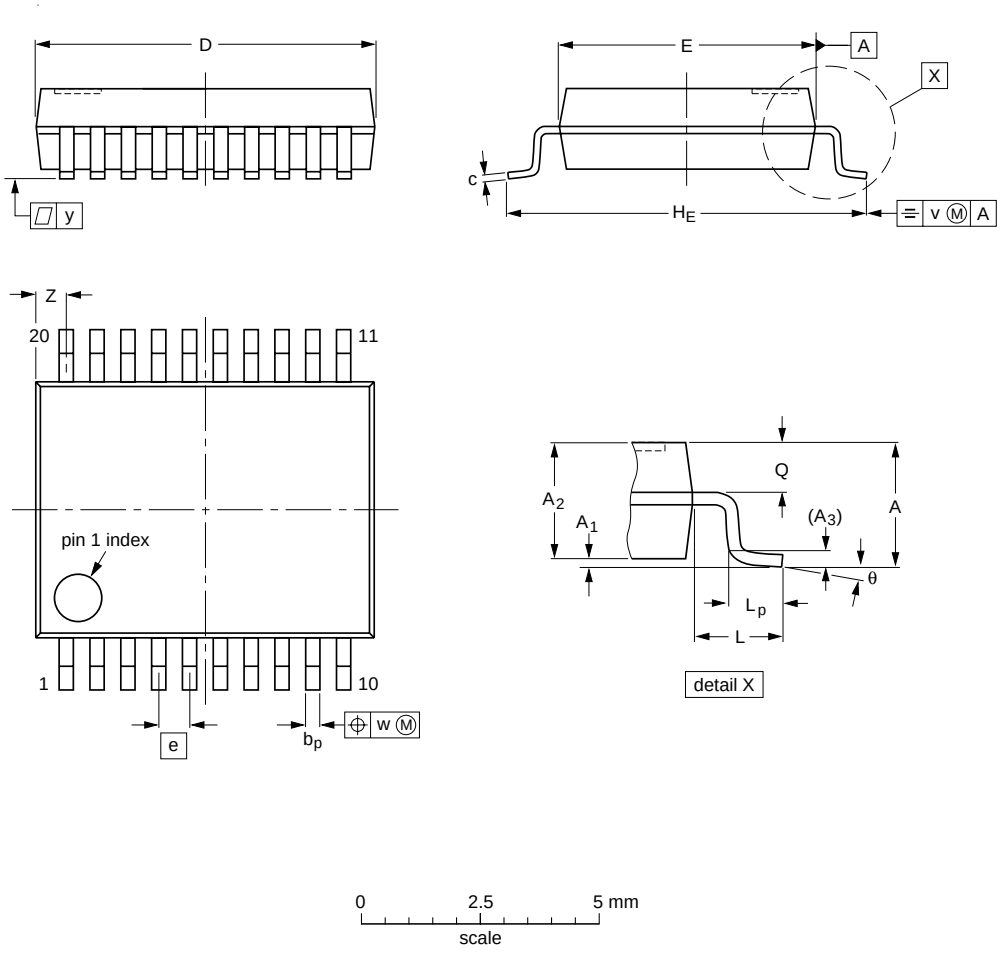
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 7. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

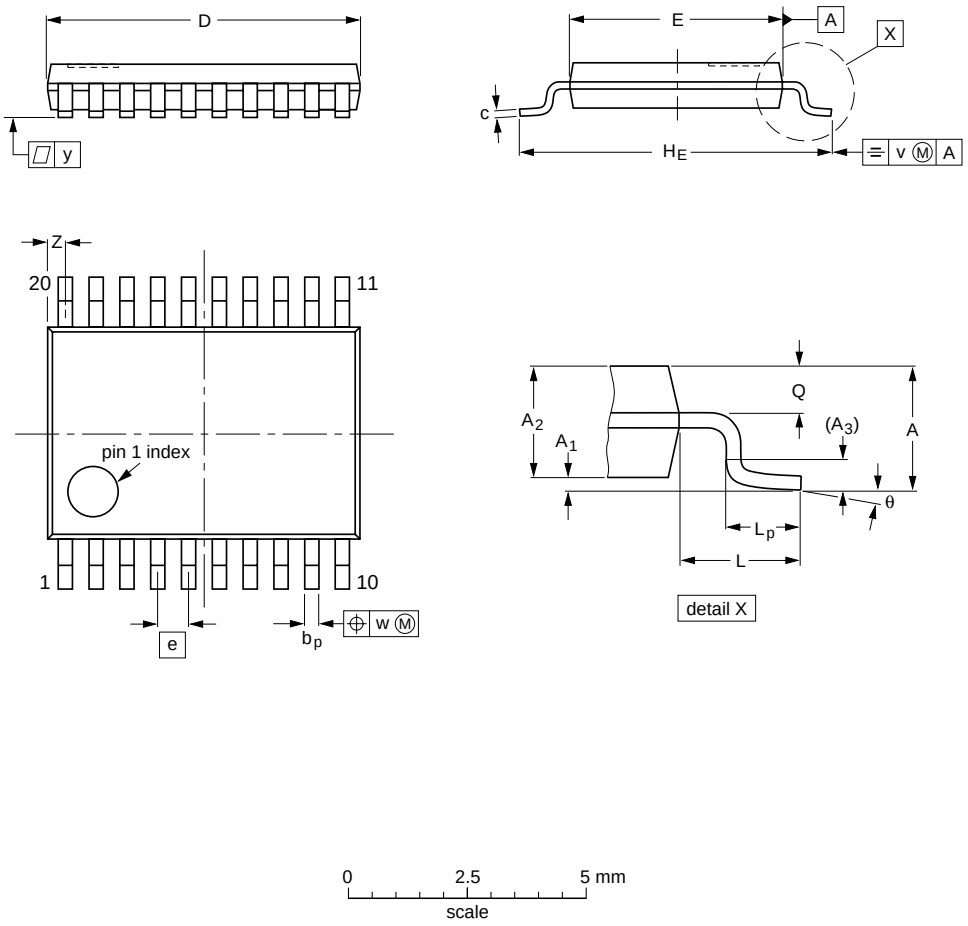
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Fig 8. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT360-1 (TSSOP20)

14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVC377_5	20050221	Product data sheet	-	9397 750 14589	74LVC377_4
Modifications:	• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors. • Table 8 “Dynamic characteristics”: changed maximum values of propagation delay t_{PHL} and t_{PLH} at T_{amb} = –40 °C to +125 °C and 2.7 V from 7.9 ns into 10.0 ns and at 3.0 V to 3.6 V from 7.6 ns into 9.5 ns.				
74LVC377_4	20040528	Product specification	-	9397 750 10615	74LVC377_3
74LVC377_3	20021023	Product specification	-	9397 750 10513	74LVC377_2
74LVC377_2	19980729	Product specification	-	9397 750 04508	74LVC377_1
74LVC377_1	19960606	Product specification	-	-	-

15. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

16. Definitions

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18. Contact information

For additional information, please visit: **http://www.semiconductors.philips.com**

For sales office addresses, send an email to: **sales.addresses@www.semiconductors.philips.com**

19. Contents

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